

The diagram shows a pixel circuit 100. A scanning line 102 is connected to the gate of TFT1 106. A data line 104 is connected to the gate of TFT2 110 and the source of TFT1. The source of TFT2 is connected to the gate of TFT1. The drain of TFT1 is connected to a capacitor C 108 and the source of TFT2. The drain of TFT2 is connected to an OLED 104 and the source of TFT1. The circuit is powered by VDD and VSS.

FIG. 1 (PRIOR ART)

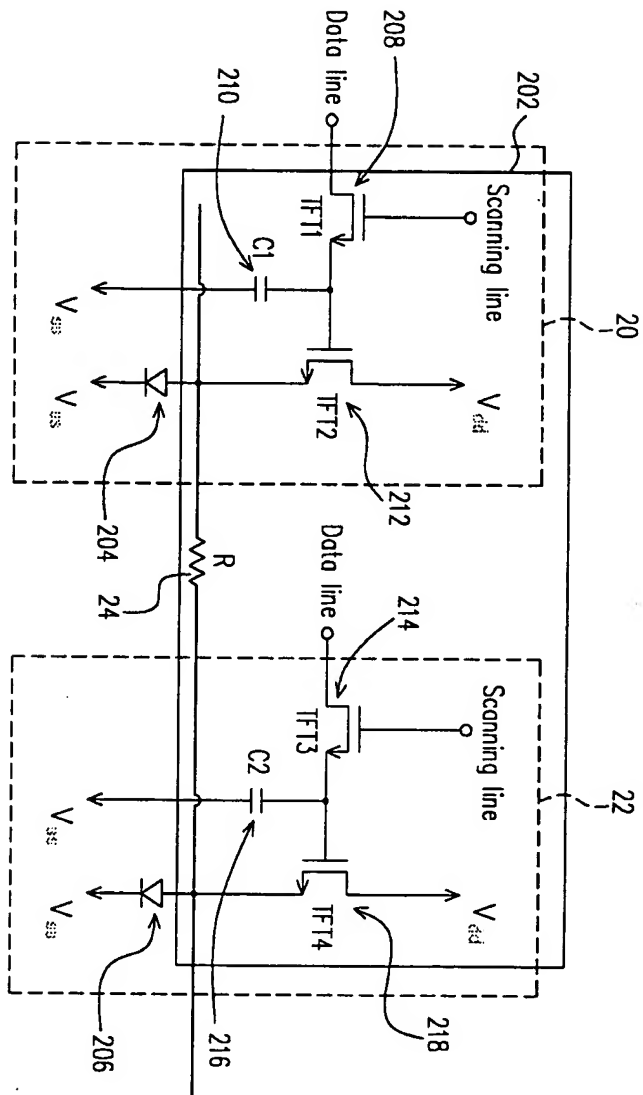


FIG. 2